

Voltage Overstress Protection in CMOS ICs

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- **Introduction**
- **Overview of technologies**
- **Problem description**
- **Schematic approaches**
- **Proposed solutions**
- **Level shifter design**
- **USB Full-Speed driver architecture**
- **Lifetime calculations**
- **Conclusion**

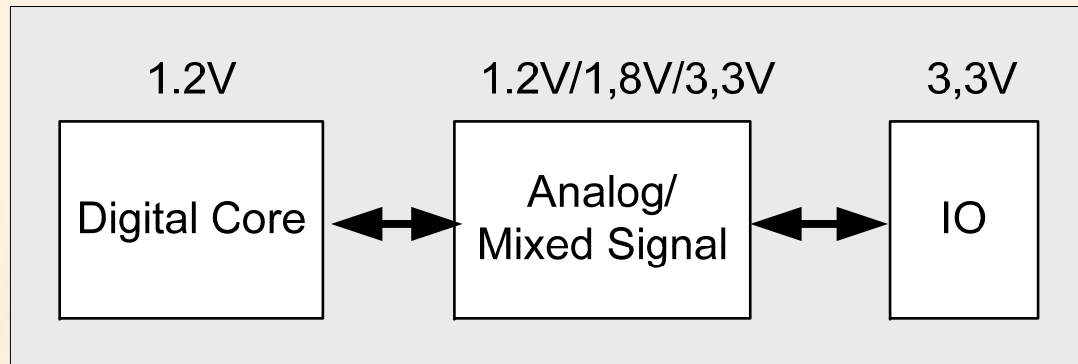
- **Continuing technological shrinkage brings to lowering allowed maximum voltages applied to MOS devices and IC supply voltages**
- **High voltages applied to CMOS devices:**
 - devices' failures
 - parametrical degradation over the time
- **Physical phenomenon causing MOS degradation/failure**
 - HCI – Hot Carrier Injection
 - NBTI – Negative Bias Temperature Instability
 - TDDB – Time Dependent Dielectric Breakdown
 - SILC – Stress Induced Leakage Current
- **Device performance time can be increased either by improving technological processes or using newer approaches in circuit designs**

Technology	Thick oxide transistors		Thin oxide transistors	
	Supply Voltage (V)	T _{ox} (nm)	Supply Voltage (V)	T _{ox} (nm)
130nm	2,5 V	~5,8	1,5	~3,3
90nm	2,5	~5,7	1,2	~2,6
65nm	2,5/1,8	~5,6/~3,6	1..1,2	~2,4
45nm	2,5/1,8	~5,5/~3,4	0,9..1,1	~2..2,3
32nm(HK-MG)	2,5/1,8	~8,6/~5,9	0,9..1	~3,2

- Usually max allowed voltage over MOS two different nodes is VDD+20%

- Many widespread IO standards (USB, PCI, etc.) use 3,3V supply

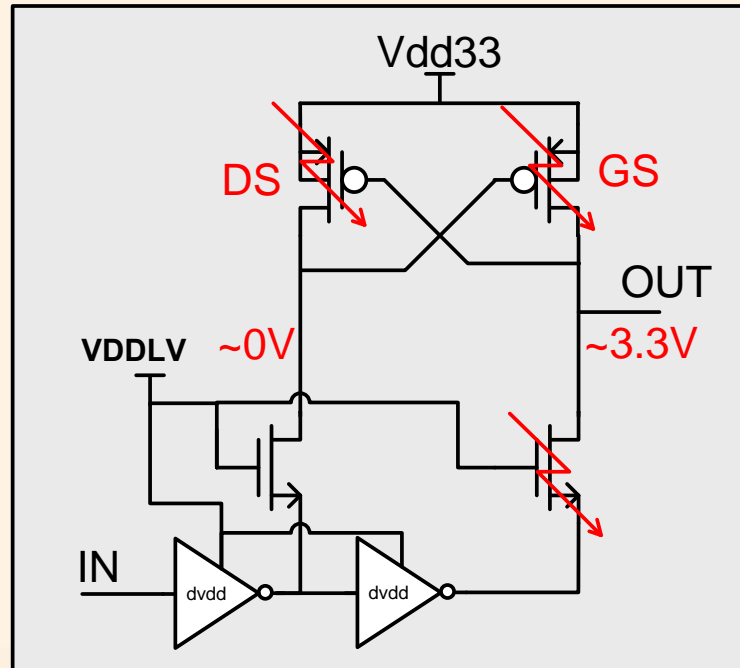
USB/PCI PHY



- **Most susceptible blocks to overstress**
 - Level Shifters. Transition from low voltage to high voltage domain
 - IO cells. Wide swing signaling with low voltage devices
- **Benefits**
 - Gain in area/performance – low cost/power
 - No need in additional mask – low cost
- **Drawbacks**
 - Reliability issues under high voltage operation

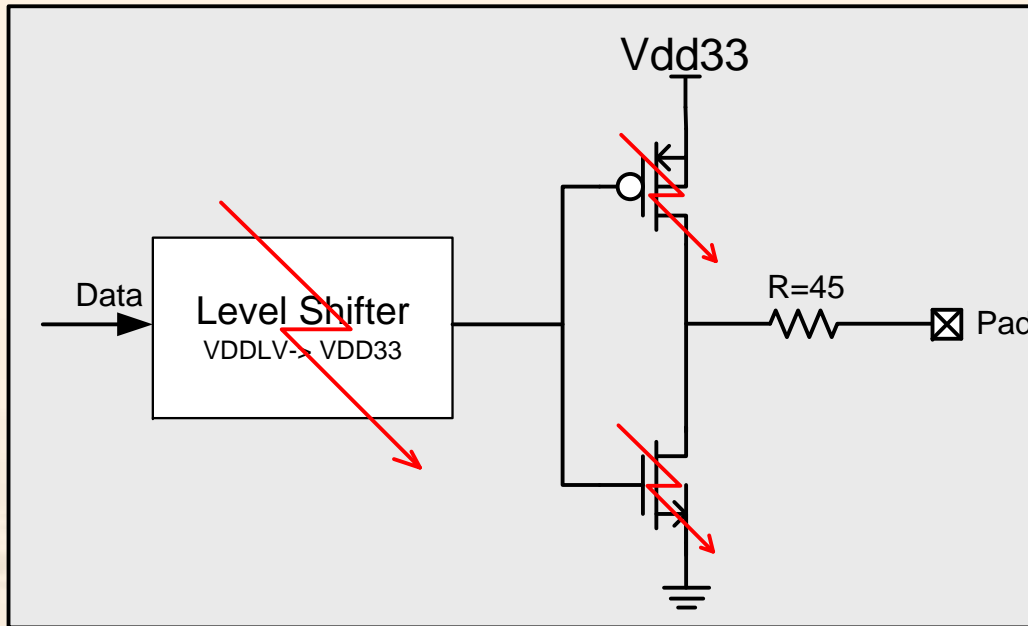
Overstress Issue

Conventional Level Shifter



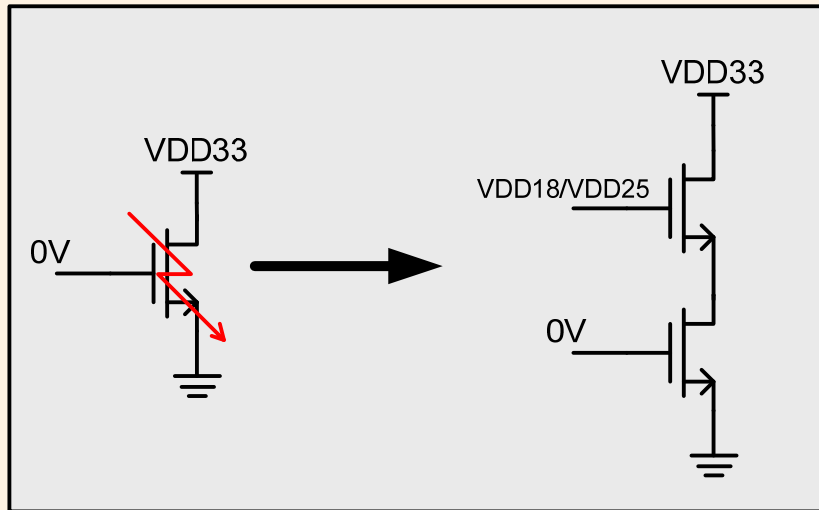
- Conventional Level-Shifter is appropriate with 3.3V devices
- Neither 2.5V nor 1.8V devices can sustain overstresses with this schematic

USB FS driver's conventional architecture



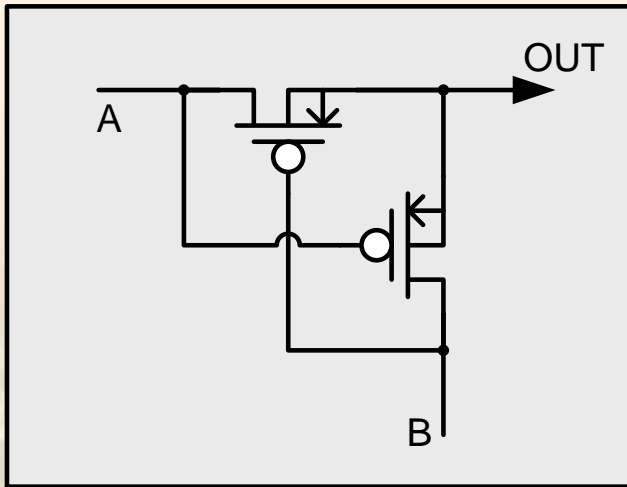
- Conventional design is suitable for 3.3V devices
- Overstress issues with 2.5V nor 1.8V devices

Overstress Protection Techniques: Cascoding



- **Allows to redistribute large voltage over several series connected devices**
- **Costs area and performance**

Overstress Protection Techniques: Voltage Limitation



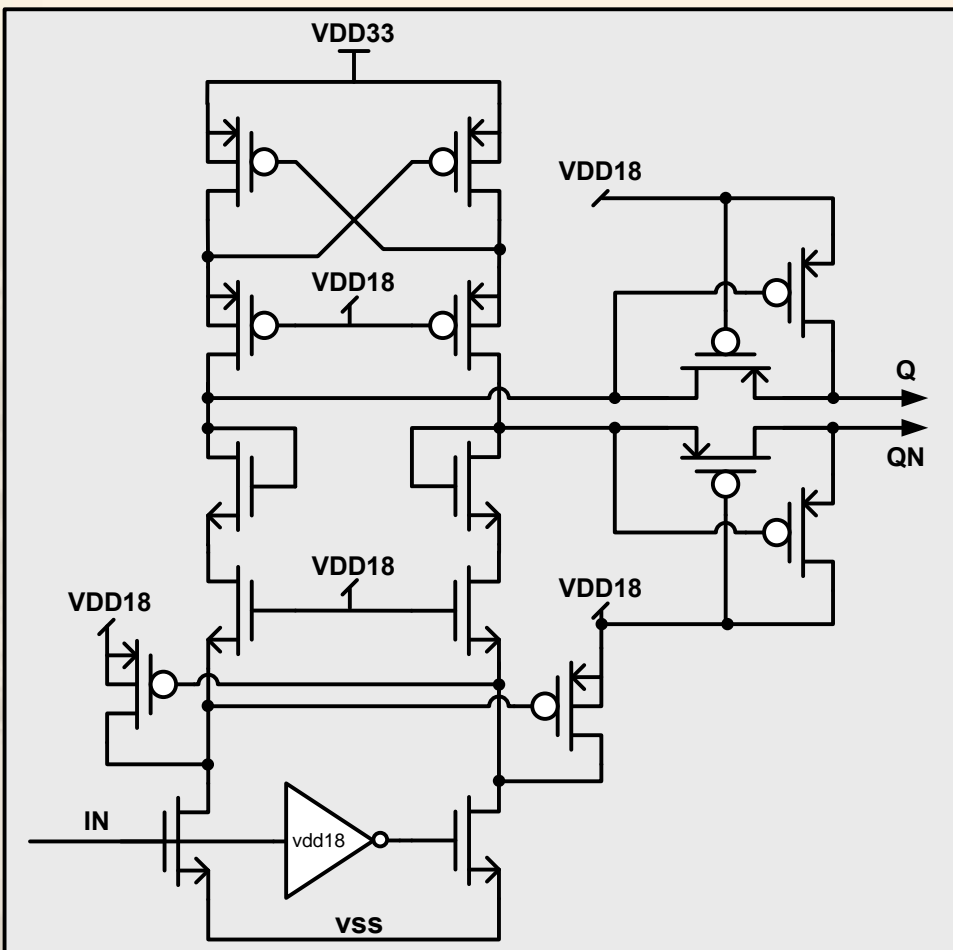
$$V(\text{OUT}) = \begin{cases} V(\text{A}), & \text{if } V(\text{A}) > V(\text{B}) \\ V(\text{B}), & \text{if } V(\text{B}) < V(\text{A}) \end{cases}$$

- $V(\text{OUT})$ chooses highest from two inputs

- Can be used as voltage limiter, if one of the inputs is set to desired minimal value
- High impedance when $|V(\text{A}) - V(\text{B})| < V_{\text{TH}}$:
 - Floating node
 - Large rise/fall times

Proposed Solution

Level Shifter Based on 1.8V Devices



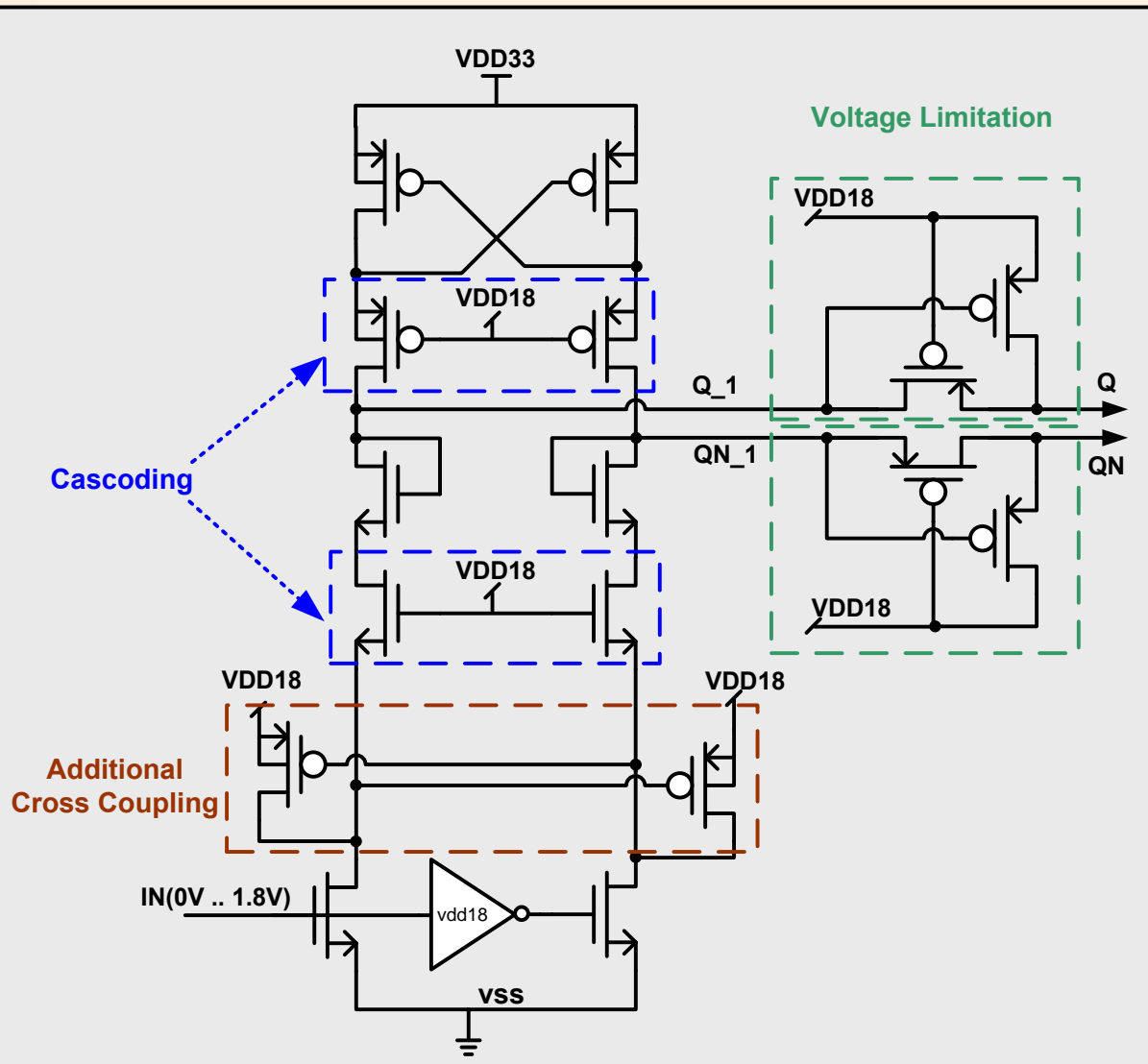
- Cascoding techniques employed for devices' overstress protection as well as positive feedback
- Circuit provides two invert outputs Q and QN with:

$$V_{LO} = VDD18$$

$$V_{HI} = VDD33$$

Proposed Solution

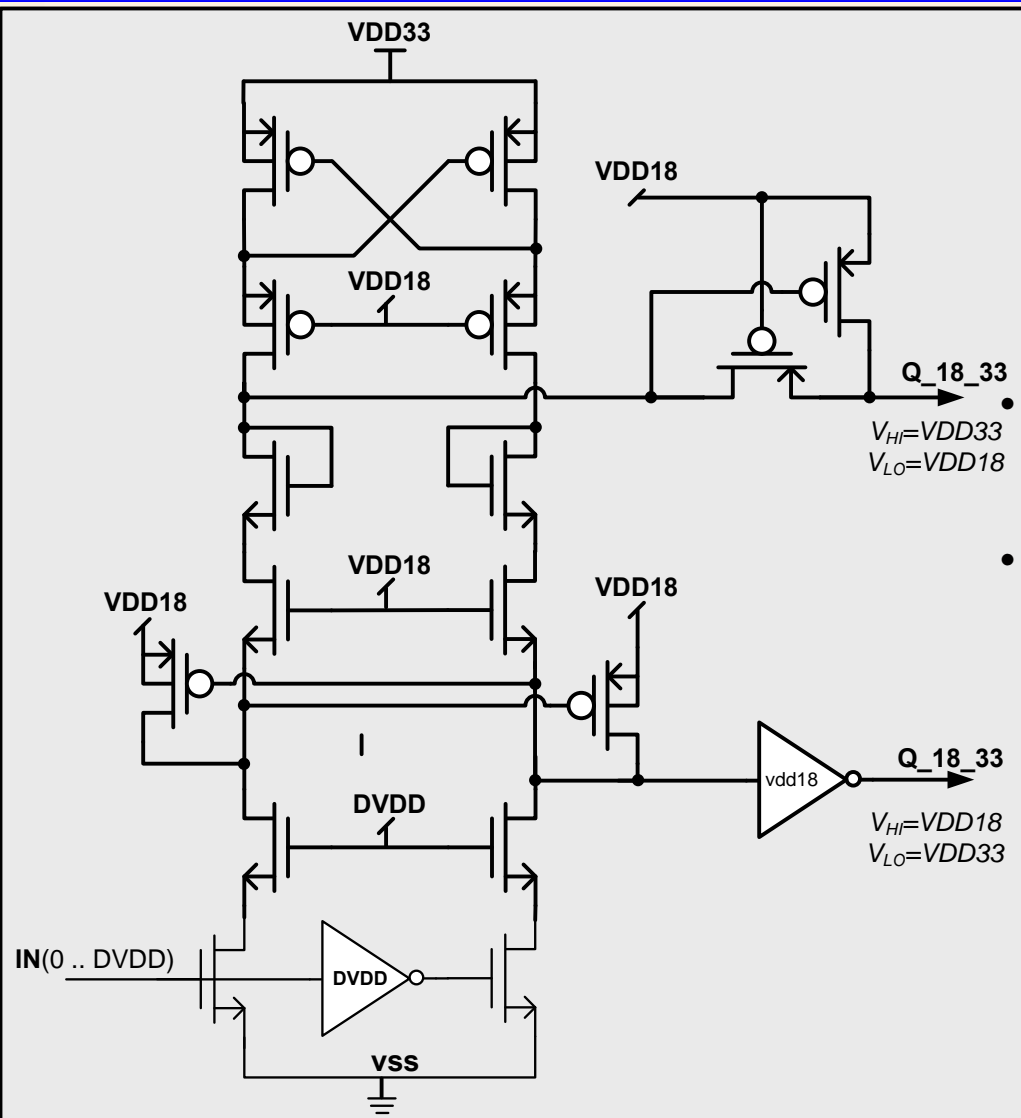
Level Shifter Based on 1.8V Devices



- Large swing on Q_1 and QN_1
 $V_{LO} = VDD18$
 $V_{HI} = VDD33$
- Additional cross coupling improves performance and relieves overstress

Proposed Solution

Dual output Level Shifter

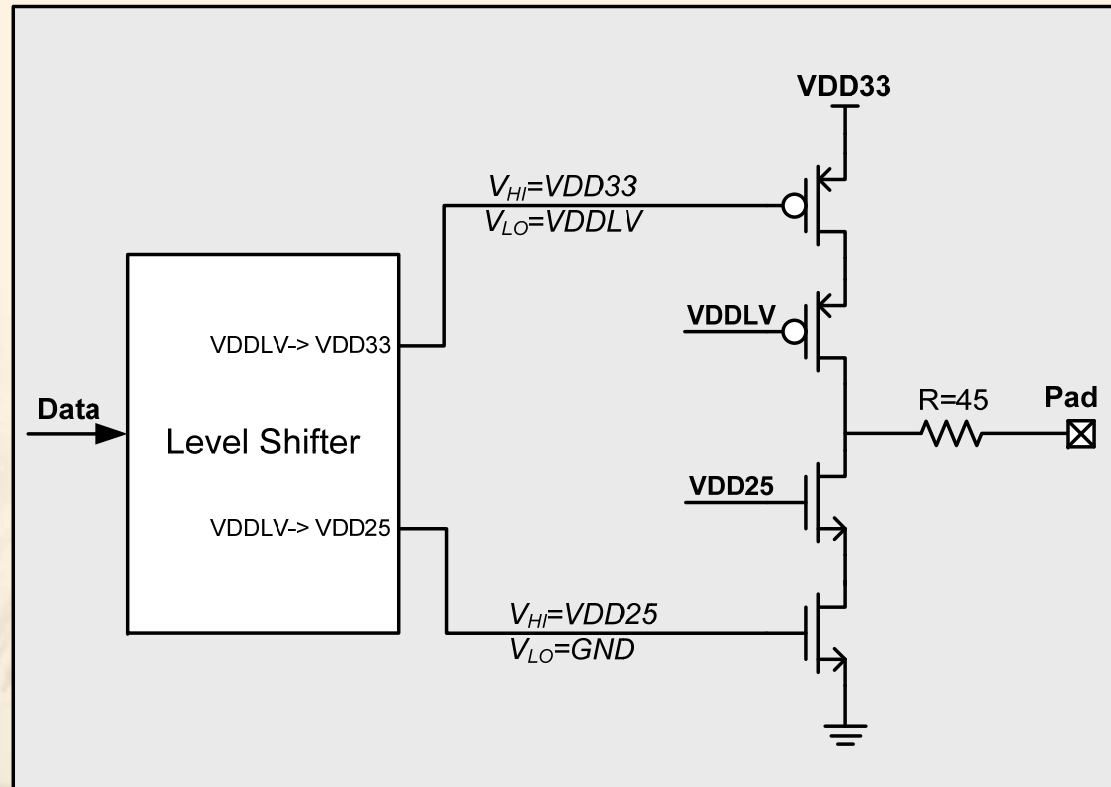


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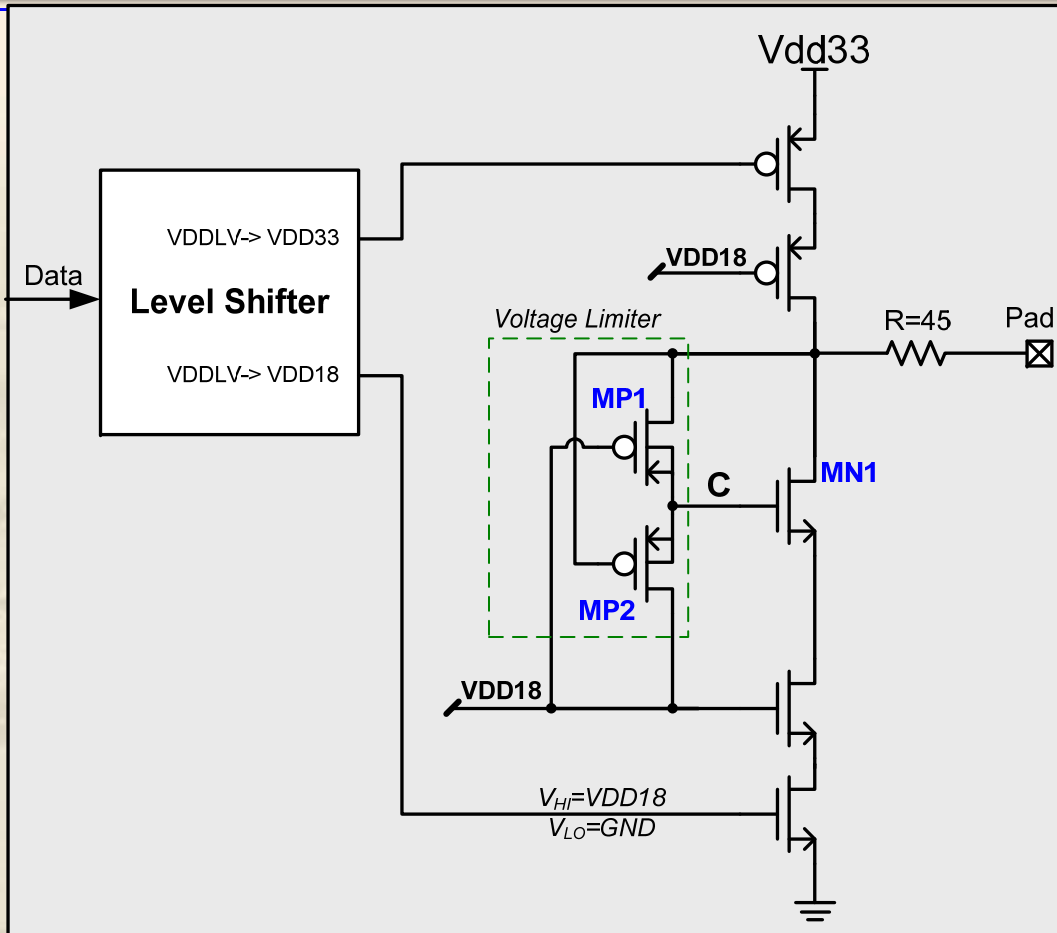
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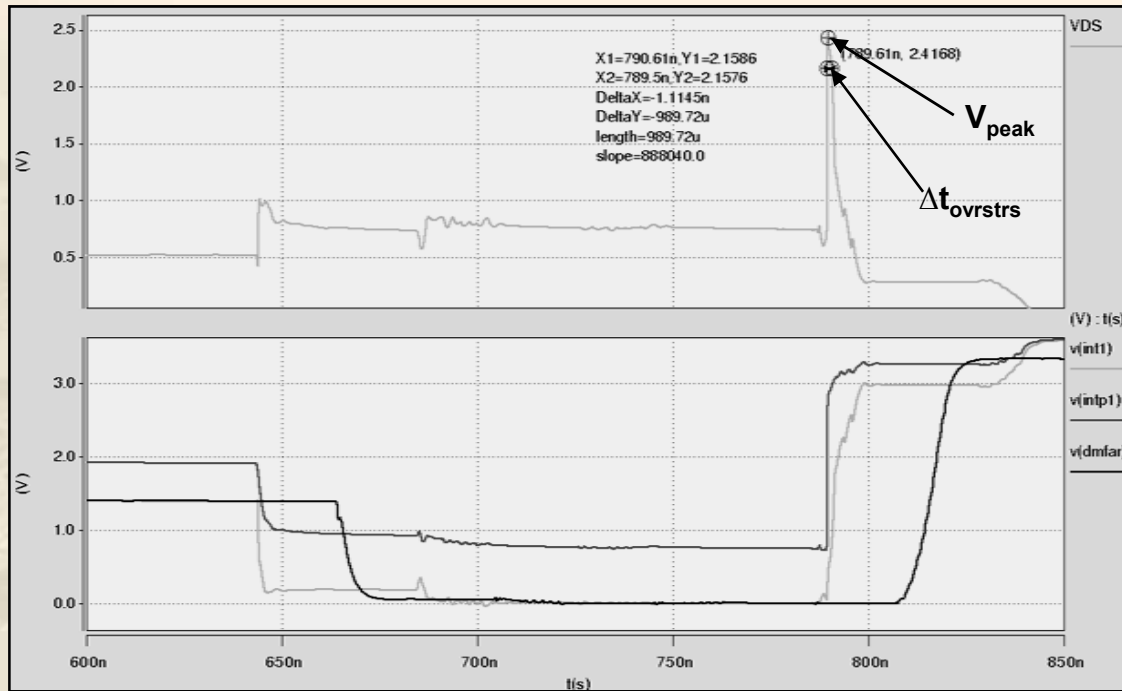


- Cascoding techniques used for redistributing large voltage over two devices.



- **Additional cascoding with MN1 provides overstress protection when $V(pad)=3.3V$**
- **MP1 and MP2 provide following function:**

$$V(C) = \begin{cases} V(pad), V(pad) > VDD18 \\ VDD18, V(pad) < VDD18 \end{cases}$$



$$T_{\text{life}} = T_{\text{life_DC}} / (\Delta t_{\text{ovrstrs}} * F)$$

T_{life} - overstressed device lifetime

$T_{\text{life_DC}} = f(V_{\text{peak}})$ - device lifetime under DC overstress

$\Delta t_{\text{ovrstrs}}$ - overstress duration

F - frequency of repetition

- Simple in calculation
 - No need to taking into account overstress voltage variation during the time
- Pessimistic
 - Takes into account the maximal overstress voltage V_{peak}

- Cascoding as a method of voltage distribution over several devices
- Voltage limitation circuit for preventing from wide voltage swing and controlling gates of additional cascodes
- Proposed USB FS driver configuration and Level-Shifter design based on 2.5V and 1.8V devices with lifetime >10yrs.
- Level-shifter and USB FS driver designs are silicon proven



Thank you