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TIQ Based Analog to Digital Converters and Power Reduction Principles

Final Report by
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1. Introduction

At present, there exists a variety of ADCs with different architectures, resolutions, sampling rates, power consumptions, and temperature ranges. These ADCs are used in different applications from mobile communication devices to measure equipment. Since the performance sampling rate, resolution, and power consumption of an ADC is basically determined by its architecture, one single ADC type cannot cover all applications. Therefore, it is important to properly choose an ADC for each particular application.

For instance, flash (parallel) ADCs can be used in high speed and low resolution applications. On the other hand, a successive approximation ADC can be used in low-speed and high-resolution applications since the conversions are done in many cycles with only one comparator. The pipelined ADC can operate at a high speed, but it is slower than the flash. The ADCs are used for high resolution and low speed applications Fig1.

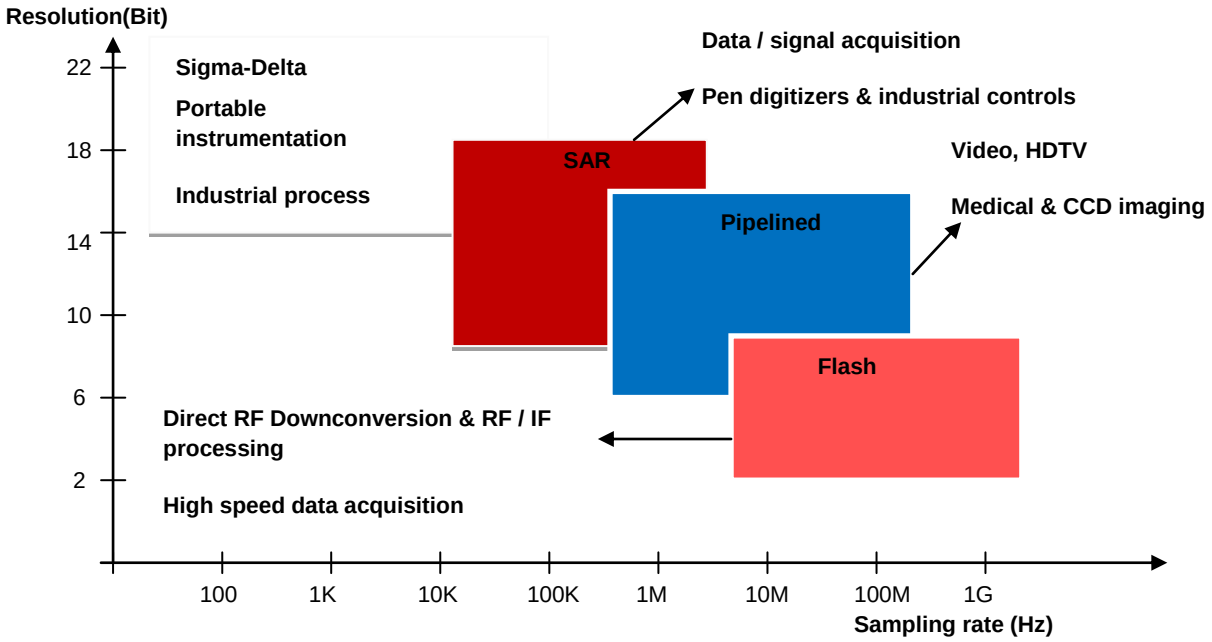


Fig. 1

2. Flash ADC structure

Each comparator has a reference voltage that is provided by an external reference source. These reference voltages are equally spaced by VLSB. An analog input is

connected to all comparators so that each comparator output is produced in one cycle. The digital output of the set of comparators – called the thermometer code is changed

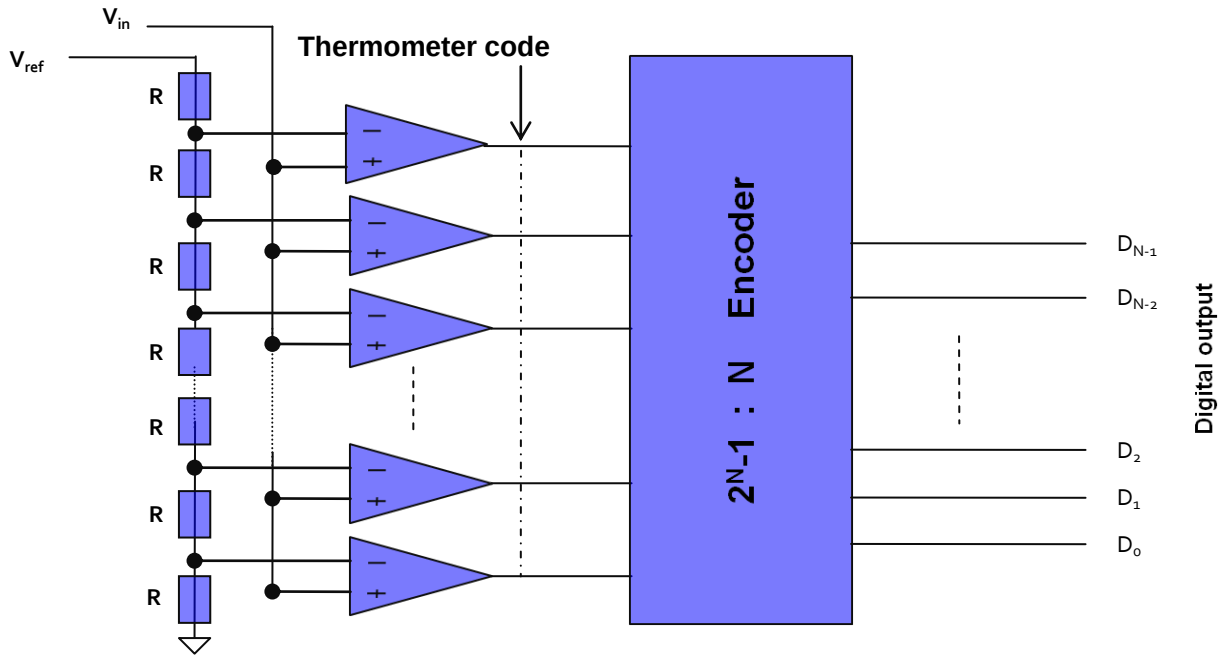


Fig. 2

into a binary code through the encoder Fig2. The flash ADC architecture has high speed

conversion due to its parallel structure. However, the flash ADC needs a large number of comparators as the resolution increases. This exponentially increasing number of comparators requires a large die size and a large amount of power consumption.

3. TIQ Flash ADC

The use of two cascading inverters as a voltage comparator is the reason for the technique's name. The voltage comparators compare the input voltage with internal reference voltages, which are determined by the transistor sizes of the inverters. Hence, we do not need the resistor ladder circuit used in a conventional flash ADC. The gain boosters make sharper thresholds for comparator outputs and provide full a digital output voltage swing. The comparator outputs - the thermometer code are converted to a binary code in two steps through the `01' generator and the encoder Fig 3.

Comparators role is to convert an input voltage (Vin) into a logic `1' or `0' by comparing a reference voltage (Vref) with the Vin. If Vin is greater than Vref , the output of the comparator is `1', otherwise `0'. The TIQ comparator uses two cascading CMOS inverters as a comparator for high speed and low power consumption.

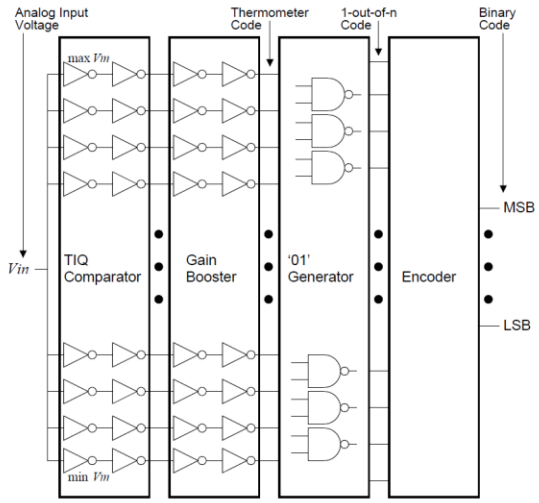


Fig. 3

The inverter threshold (Vm) is defined as the Vin = Vout in the VTC of an inverter.

$$V_m = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}\left(V_{DD} - \left|V_{Tp}\right|\right) + V_{Tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}$$

The second inverter is used to increase voltage gain and to prevent an unbalanced propagation delay. With a fixed length of the PMOS and NMOS devices, we can get desired values by increasing only the width of the PMOS and NMOS transistors, respectively we assume that both transistors are in the active region, the gate oxide thickness (Cox) for both transistors is the same, and the lengths of both transistors (Lp and Ln) are also the same. We know that Vm is shifted depending the transistor width ratio (Wp/Wn). That is, increasing Wp makes Vm larger, and increasing Wn results in Vm being smaller on the VTC Fig 4.

However, to use the CMOS inverter as a voltage comparator, we should check the sensitivity of Vm to other parameters, which are ignored in, for correct operation of the TIQ flash ADC. In a mixed-signal design, the ignored parameters - threshold voltages of both transistors, electron and hole mobility, and power supply voltage - are not fixed at a constant value.

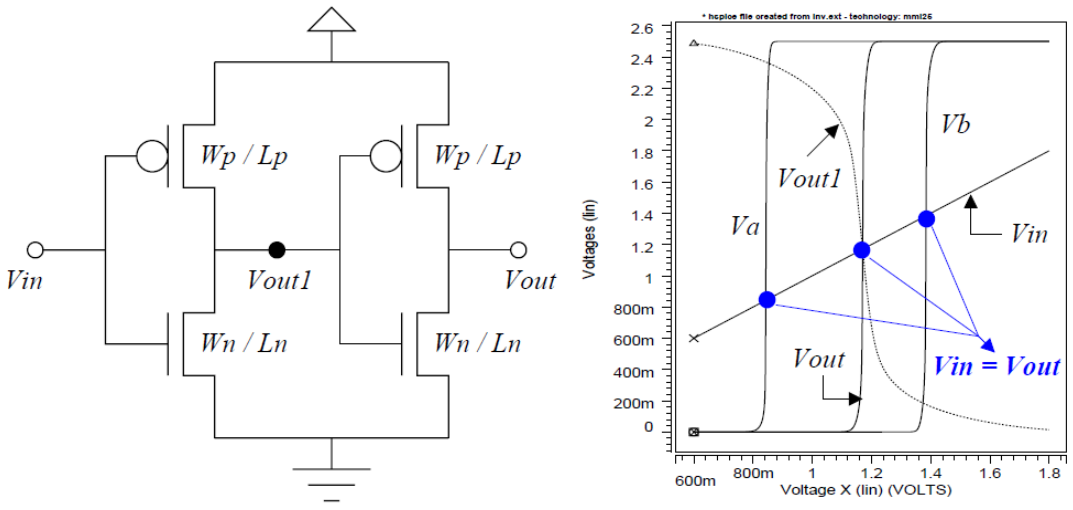


Fig. 4

The inverter threshold voltage also depends on temperature according to the following partial differential equation. If the temperature is changed, then the effective mobility, channel length, and threshold voltage of the PMOS (VTp) and NMOS (VTn) devices will be affected.

$$\frac{\partial V_m}{\partial T} = \frac{1}{1+\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}} \left(\frac{dV_{Tn}}{dT} - \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}} d\left|V_{Tp}\right|}{dT} \right)$$

$$\frac{\partial V_m}{\partial V_{DD}} = \frac{1}{1+\sqrt{\frac{\mu_n W_n}{\mu_p W_p}}}$$

Since the CMOS inverter has a single-ended input, it is more susceptible to power supply voltage noise than the differential comparator

4. Systematic Size Variation Method

Since process parameters change from one fabrication to another fabrication, the inverter threshold voltage will change. This situation is especially one of major problems for linearity errors of the TIQ comparator that uses Vm as a reference voltage.

We us the SSV technique for designing the TIQ comparator. The SSV design technique of the TIQ comparator significantly improves the linearity of the ADC in spite of the CMOS process variation.

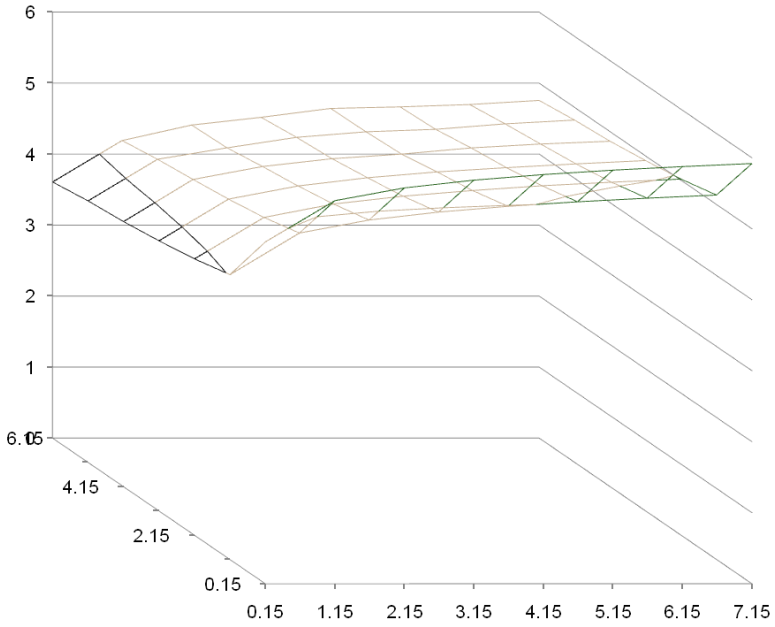


Fig. 5

A CMOS inverter consists of one PMOS and one NMOS transistor, with the inverter switching threshold voltage depending upon the transistor sizes. If one fixes the length of both the PMOS and NMOS transistors at a constant size, one can obtain different inverter threshold voltages by simply varying the transistors' widths.

In the case of the systematic size variation (SSV) technique, the Vm is selected from the 3-D plot Fig. 5.

5. Quantum Voltage Comparator

The new QV comparator has been devised from the simple tranconductance amplifier. The single-ended inverter is very sensitive to noise in both the power supply and input signal. By systematically increasing the size of transistor M3 and decreasing the size of transistor M4, each of the 2n − 1 QV comparators has a different reference voltage in descending order. Using comparator which consist of differential pair we can overcome problems with noise sensitivity. This structure is lower than simple inverter.

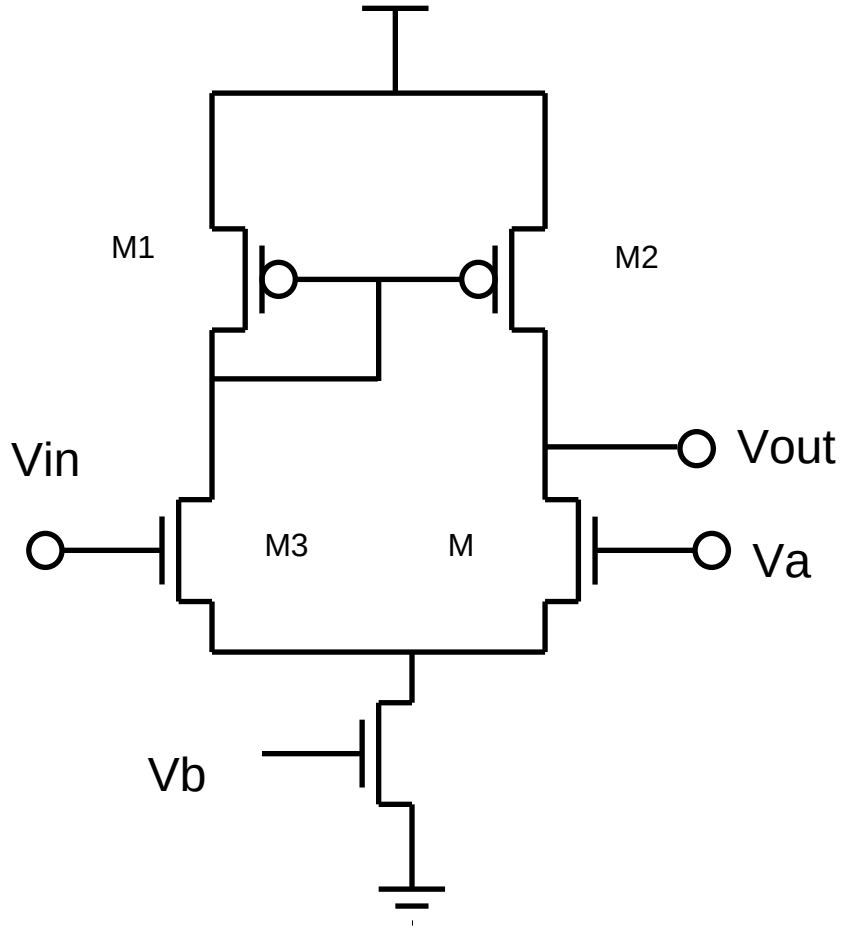


Fig. 6

6. Power Management Method

With this feature, all comparators in the ADC can be powered on when they are not used, which is called the idle period. Power dissipation in the ADC happens only at the time when the comparators are working, which is called the sampling period. Hence, the idea of this method is to control sampling intervals by adding an AND gate and a PMOS transistor. According to the logic of the AND gate, the input voltage is only sampled when both CLK and Sample are high. Input voltage is sampled once every two CLK signals (the \Read" signal is the output of the AND gate). On the other hand, if the output of the AND gate is `0', the S/H circuit will be disconnected, and the PMOS transistor that is connected to VDD will be activated. Then, the input of the TIQ flash ADC will be at the signal maximum. Therefore, there is no power consumption in the ADC during this idle period.

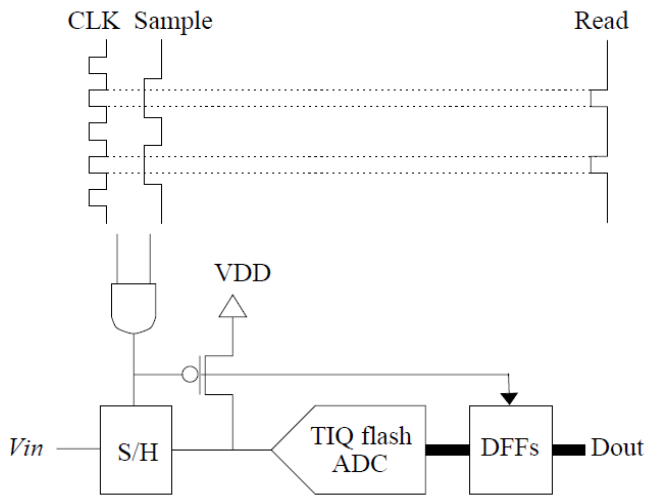


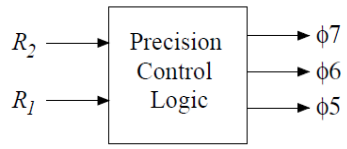
Fig. 7

7. The Power and Resolution Adaptive ADC

This feature is highly desirable in many wireless mobile applications. For example, the strength of a radio frequency (RF) signal varies greatly depending on geographic location. Optimally, the ADC resolution can be reduced upon the reception of strong signal, or the resolution can be increased upon the reception of weak signal. The substantial reduction of power consumption at lower resolution will prolong the battery-powered operation.

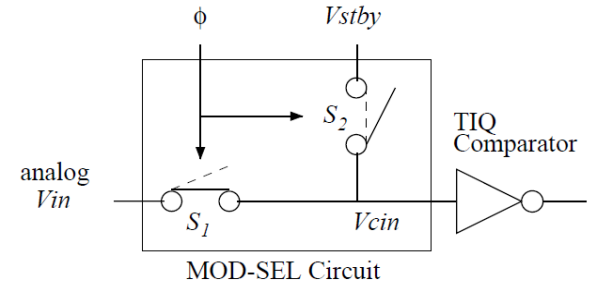
The key feature of the TIQ comparator is the fact that the comparator can easily and quickly switch from active mode to standby mode.

RA-ADC Precision	$R_2 R_1$	$\phi 7$	$\phi 6$	$\phi 5$
8-bit	0 0	1	1	1
7-bit	0 1	0	1	1
6-bit	1 0	0	0	1
5-bit	1 1	0	0	0



In the active mode, switch S1 is on and switch S2 is o, connecting the analog input signal to the TIQ comparator input. In the standby mode, S1 is o and S2 is on, connecting Vstby voltage to the TIQ comparator. The analog input signal voltage varies between GND and VDD, but the Vstby voltage is xed either to GND or to VDD. In

standby mode, the power consumption of the TIQ comparator is due to only the leakage current.



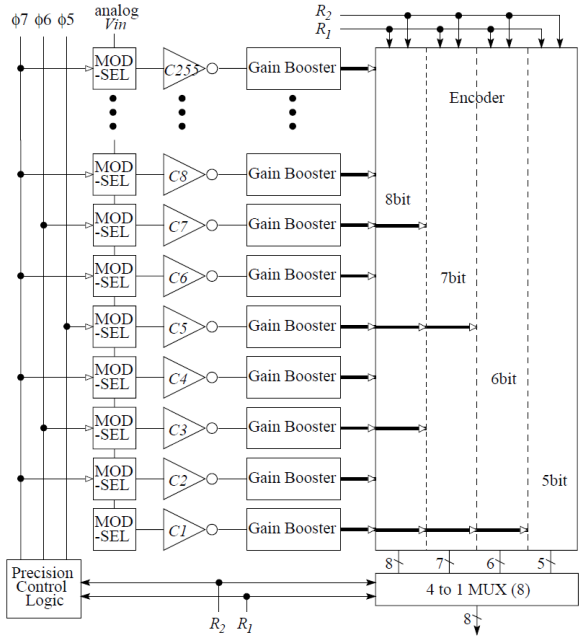


Fig. 7

When it is operating at 6-bit precision, every three out of four TIQ comparators are switched to the standby mode, achieving almost an 75% ADC power consumption reduction. Similarly a 5-bit precision results in almost 87.5% power reduction.

8. Conclusion

Because parallel voltage comparison is used in the flash ADC, the power consumption gets much larger as we increase the resolution of the ADC. With the TIQ comparator feature, we have implemented both the power and resolution adaptive flash ADC (PRA-ADC) and the power management method in the TIQ flash ADC. The PRA-ADC can operate at di_erent resolutions depending on the amplitude of a reception signal in a wireless application. Substantial reduction of power consumption at lower resolution will

prolong the battery-powered operation. The power management method can manage the power consumption by controlling its sampling interval on demand.

- Small overhead for switching
- Unused comparators go to standby mode
- Prolong the battery-powered operation
- Linear power reduction with linear frequency scaling
- Exponential power reduction with linear

  resolution reduction