# Low Voltage Bandgap References and High PSRR Mechanism

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# Outline

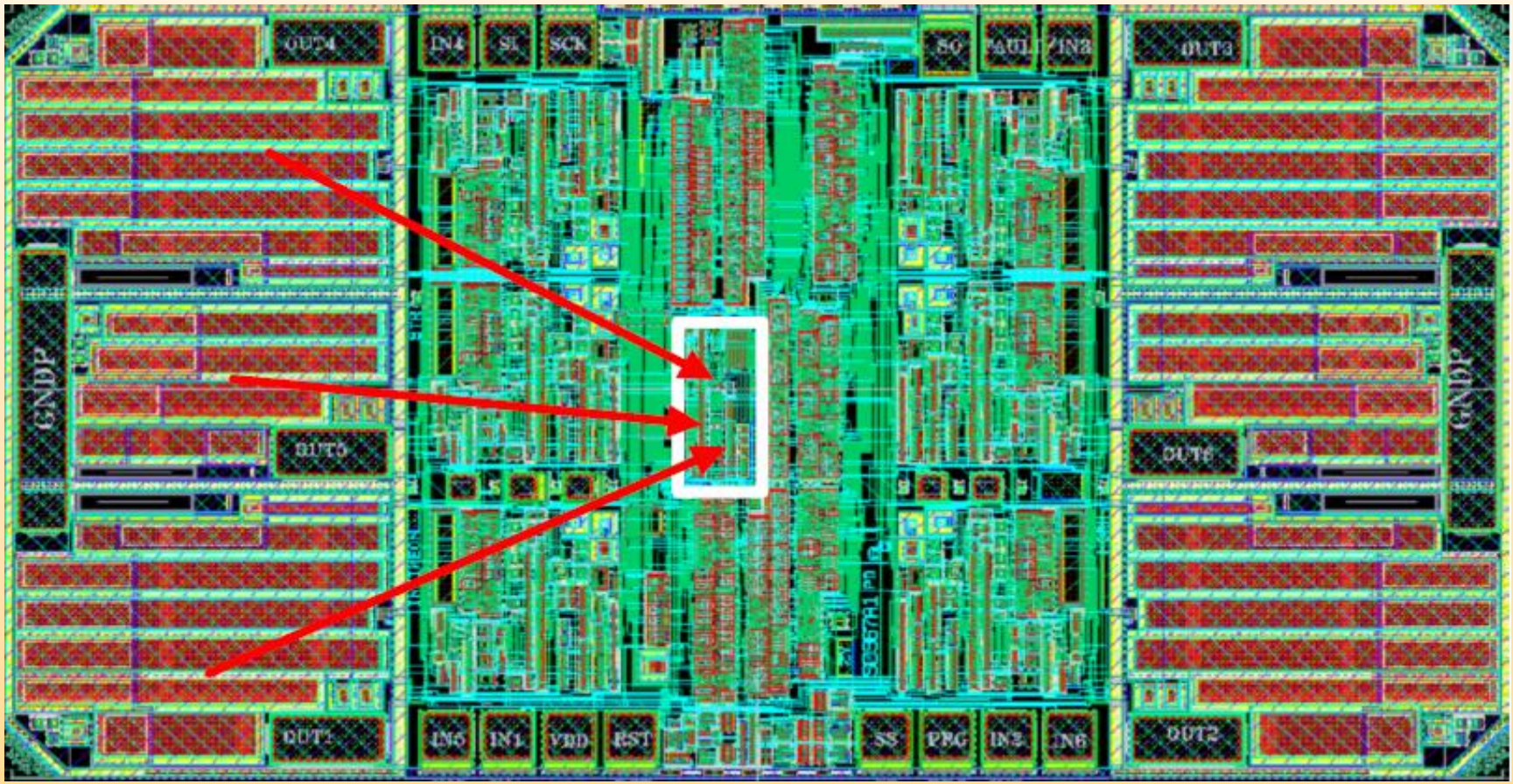
- The Necessity of Bandgap Reference
- Zener Diode References
- Enhancement and Depletion Reference
- Bandgap Reference Approach
- Implementation Using Bipolar/MOS Devices
- High PSRR Mechanism
- Simulation Results
- Conclusion

# The Necessity of Bandgap Reference

Bandgap Reference

Constant Output Voltage/Current

# BGR is an important  part of analog and mixed signal integrated circuits

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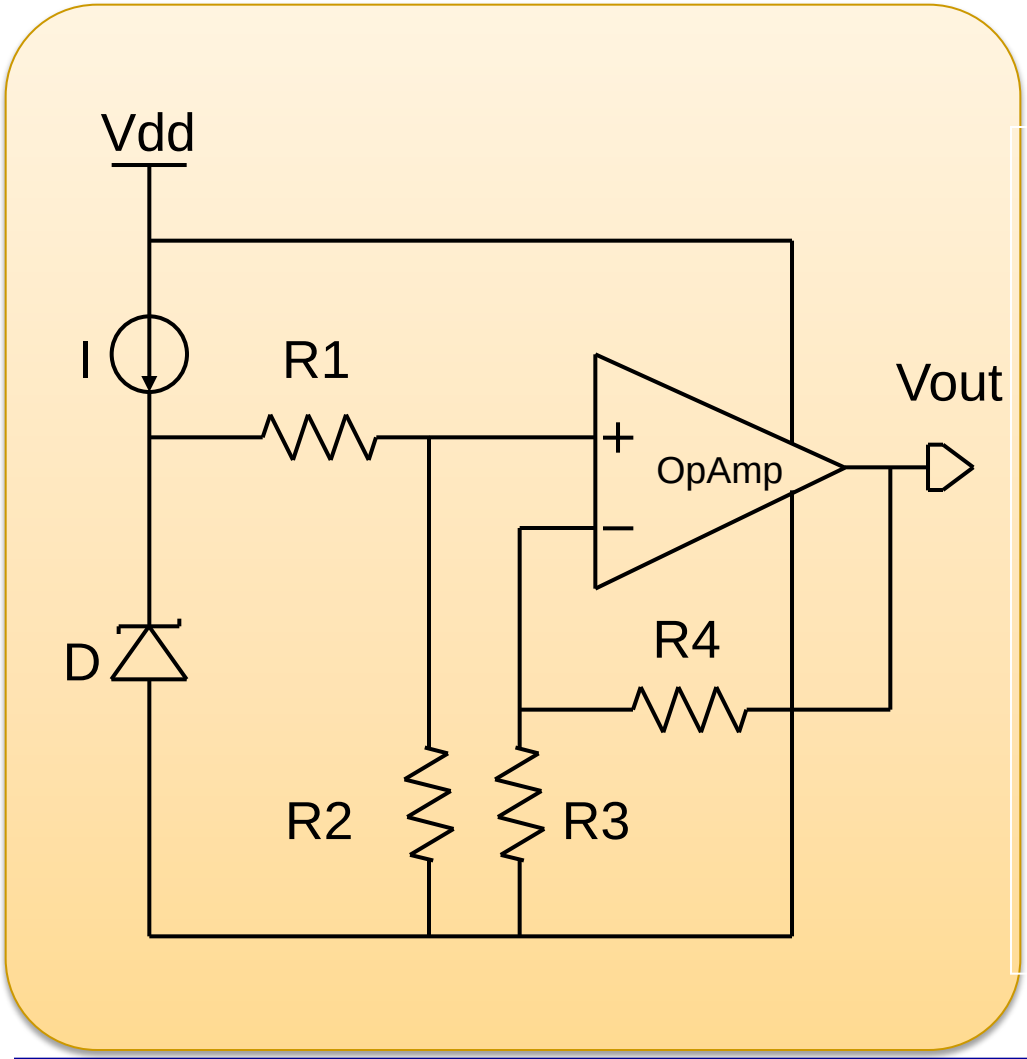
# Requirements

- Supply and Process-independent biasing
- Well defined behavior with temperature

  PVT independence

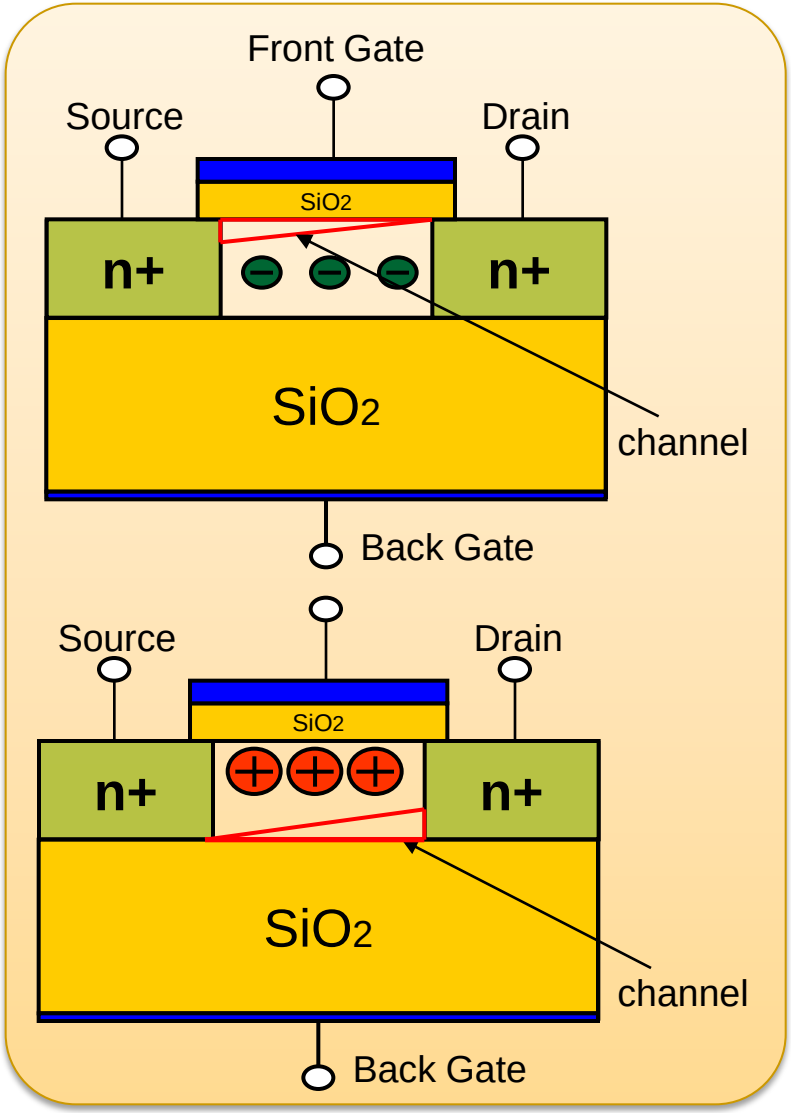
- Output noise
- Output inpedance
- Power dissipation

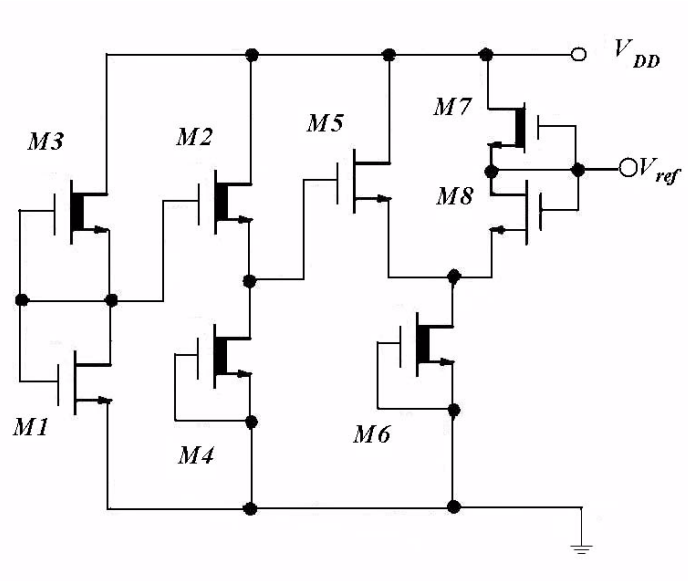
# Zener Diode References




- **Buried zener diode method**
- **Buried transistor base emitter method**

# Enhancement and Depletion Reference




$$Vref = V_{GSE} - V_{GSD} = V_{TE} + \sqrt{\frac{I_D}{K_E}} - V_{TD} - \sqrt{\frac{I_D}{K_D}}$$

$$I_D = f(T),\ K_E = \mu_E C_{ox} \frac{W}{L} = \mu_E(T) C_{ox} \frac{W}{L}$$

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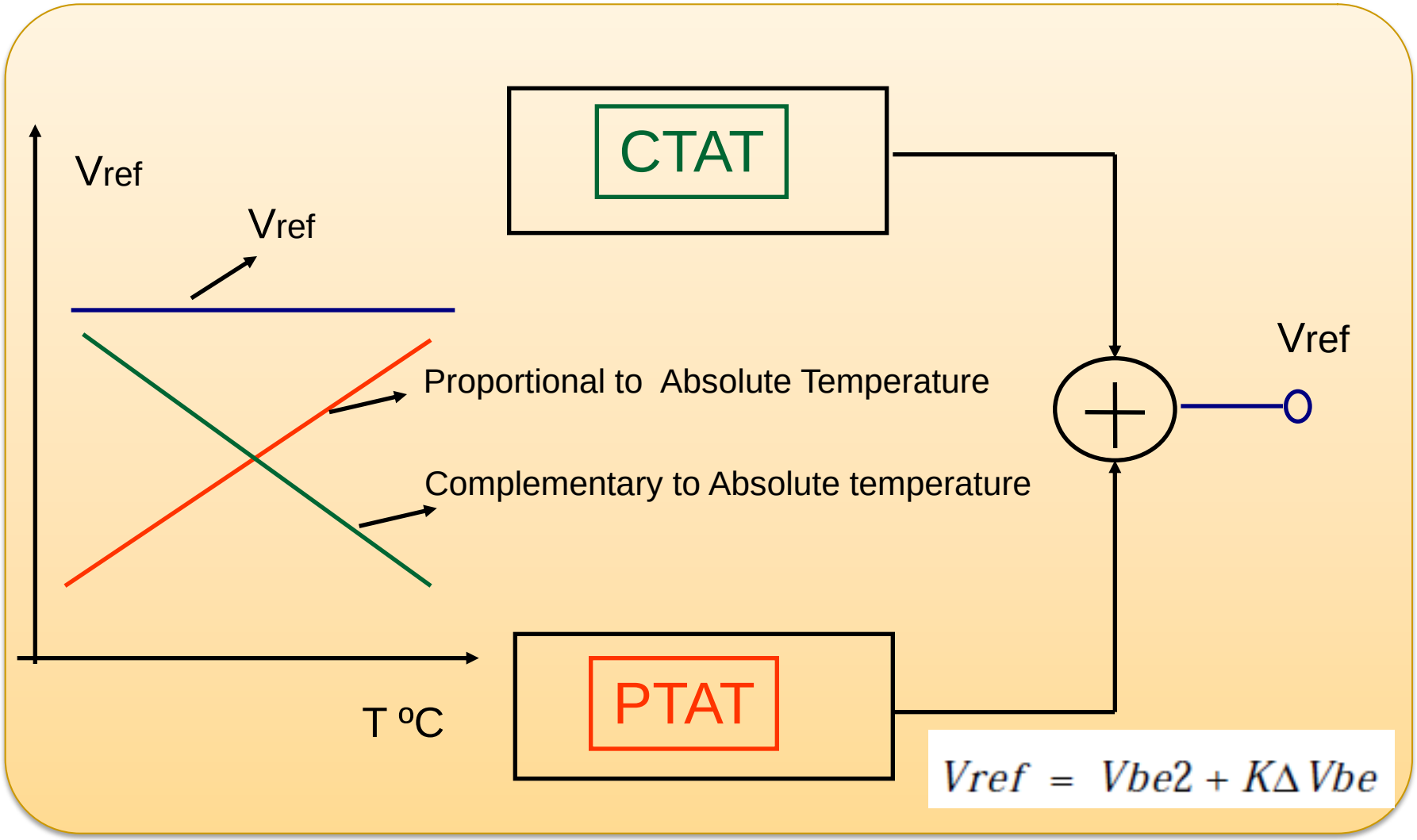
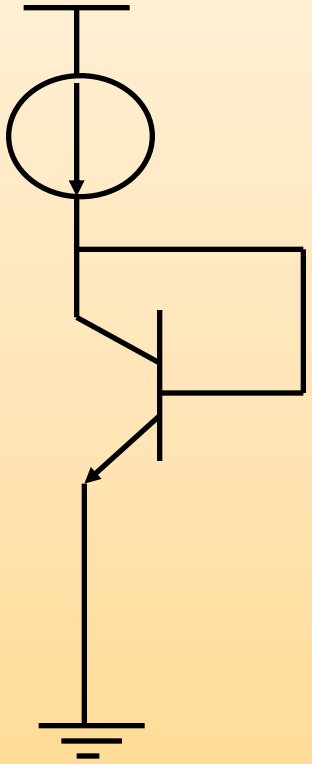
# Bandgap Reference Approach

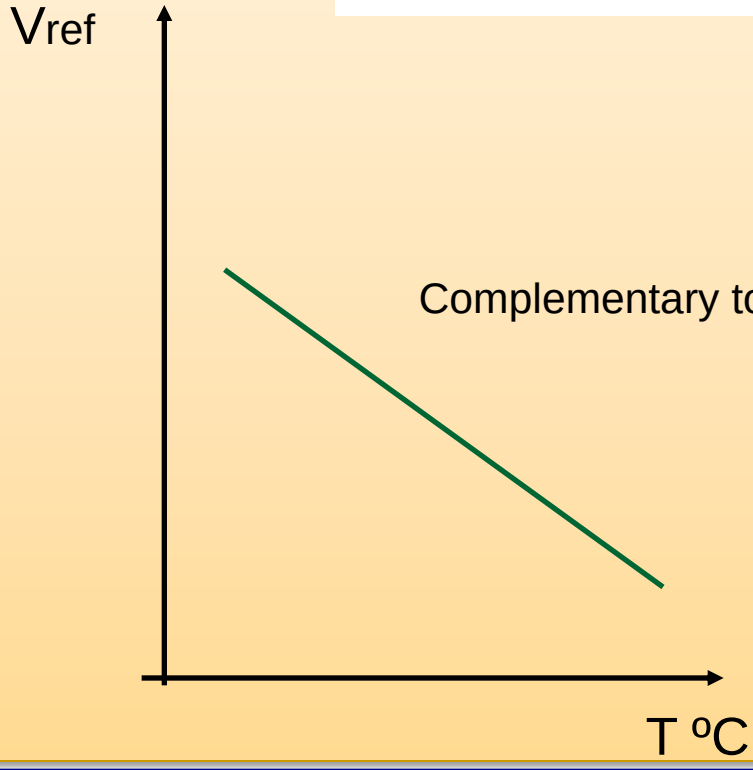


# Complimentar to Absolute Temperature CTAT

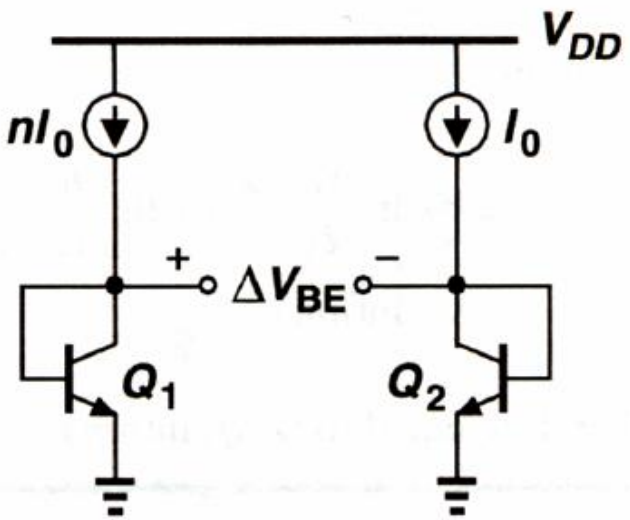
Forward-biased base-emitter junction of a bipolar transistor has an I-V relationship given by

$$I_C = I_S \, e^{qV_{BE} / kT}$$



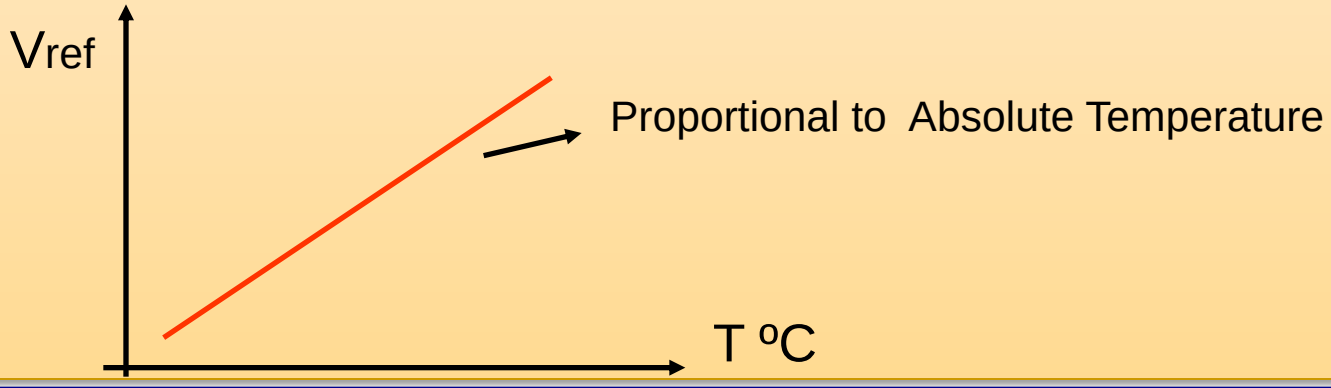


# Proportional to Absolute Temperature
# PTAT




$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$
$$= V_T \ln \frac{nI_0}{I_{S1}} - V_T \ln \frac{I_0}{I_{S2}}$$
$$= V_T \ln n.$$

PTAT voltage

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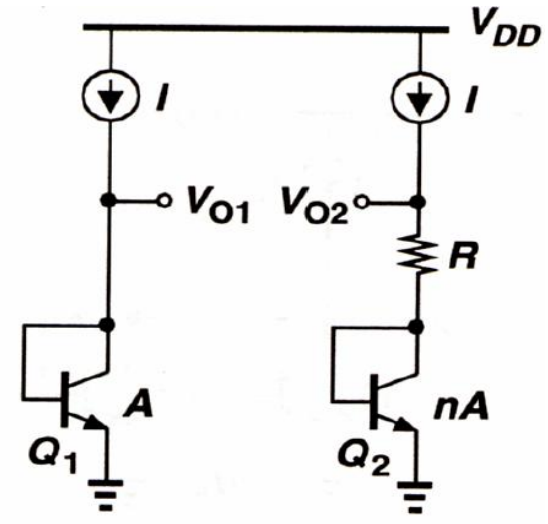
# CMOS Bandgap Reference

Bandgap reference : Vref = VBE + K VT

$$\partial V_{BE}/\partial T \approx -1.5\,\text{mV/°K}$$
$$\partial V_T/\partial T \approx +0.087\,\text{mV/°K}$$
$$V_{REF} \approx V_{BE} + 17.2V_T$$

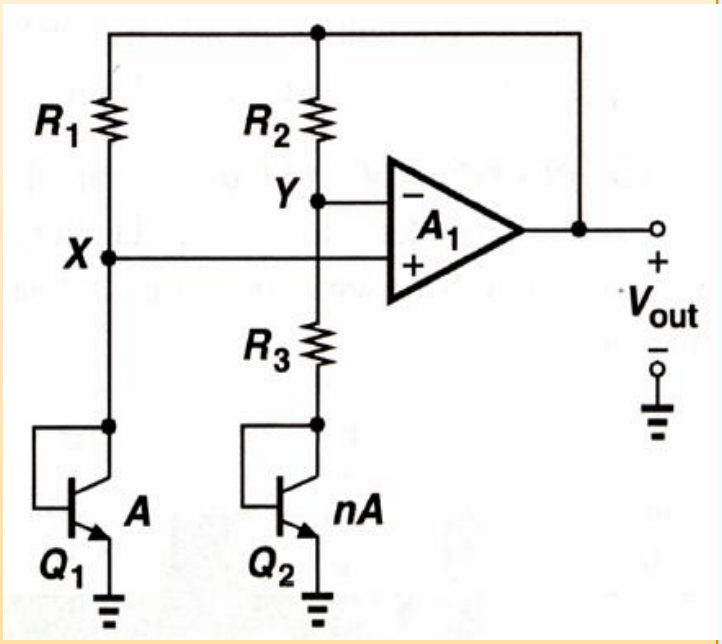



$$V_{BE1} = RI + V_{BE2}$$

$$RI = V_{BE1} - V_{BE2} = V_T \ln n$$

$$V_{o2} = R\,I + V_{BE2}$$
$$= V_T \cdot \ln n + V_{BE2}$$

# CMOS Bandgap Reference Circuit




$$V_{out} = V_{BE2} + \frac{V_T \ln n}{R_3}(R_3 + R_2)$$

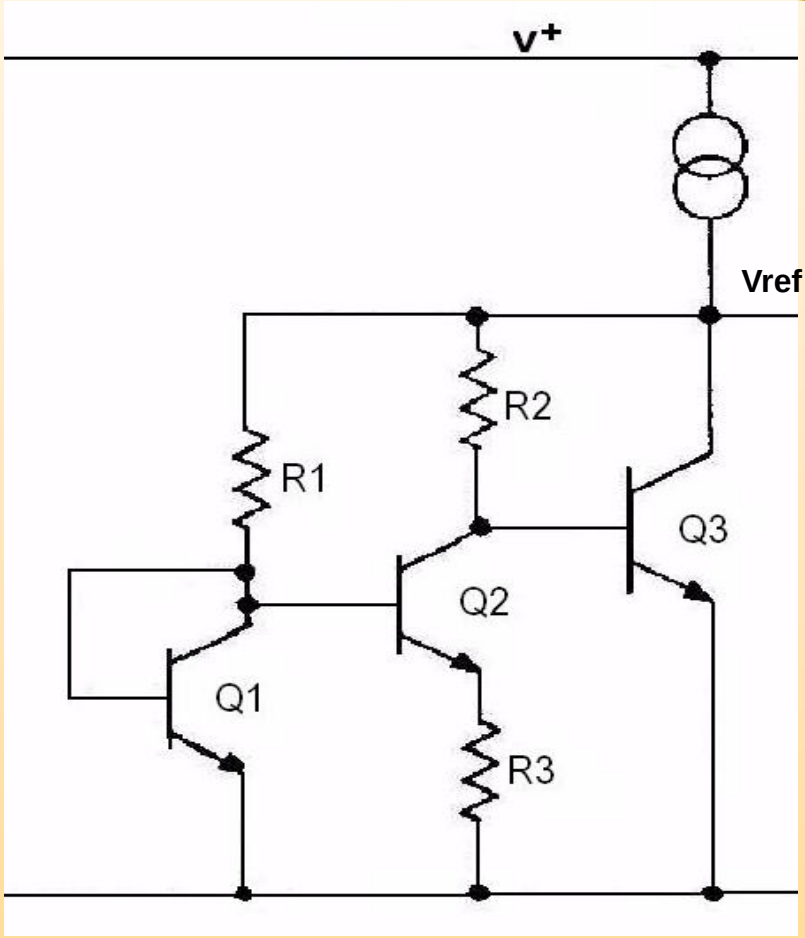
$$= V_{BE2} + (V_T \ln n)\left(1 + \frac{R_2}{R_3}\right)$$

**Actual Implementation of CMOS Band Gap Reference**

# Comparison of the Three Reference Approaches

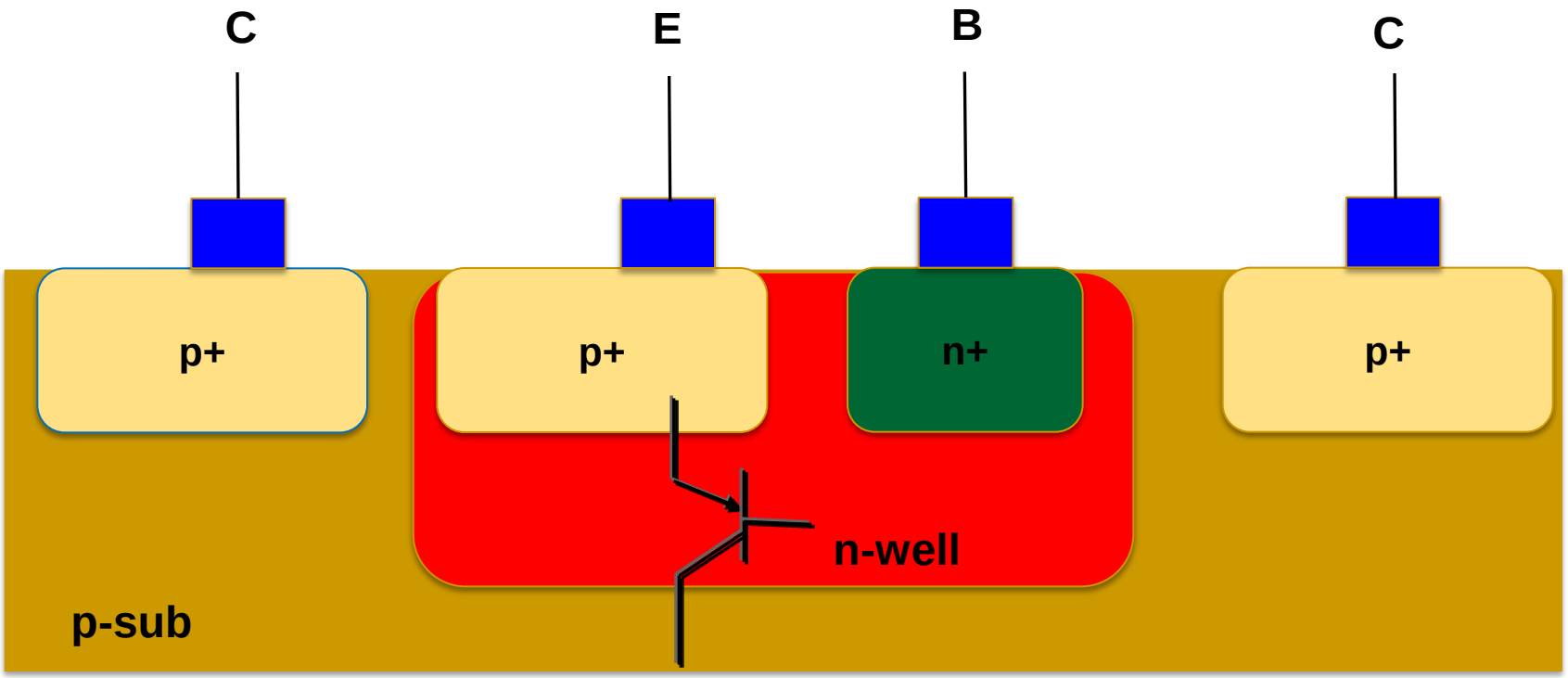
- Breakdown voltage of a zener diode is typically larger than the power supplies used in modern circuits
- In most CMOS circuits depletion transistors are not typically available
- Available in both bipolar and CMOS technologies

# Implementation Using Bipolar Devices



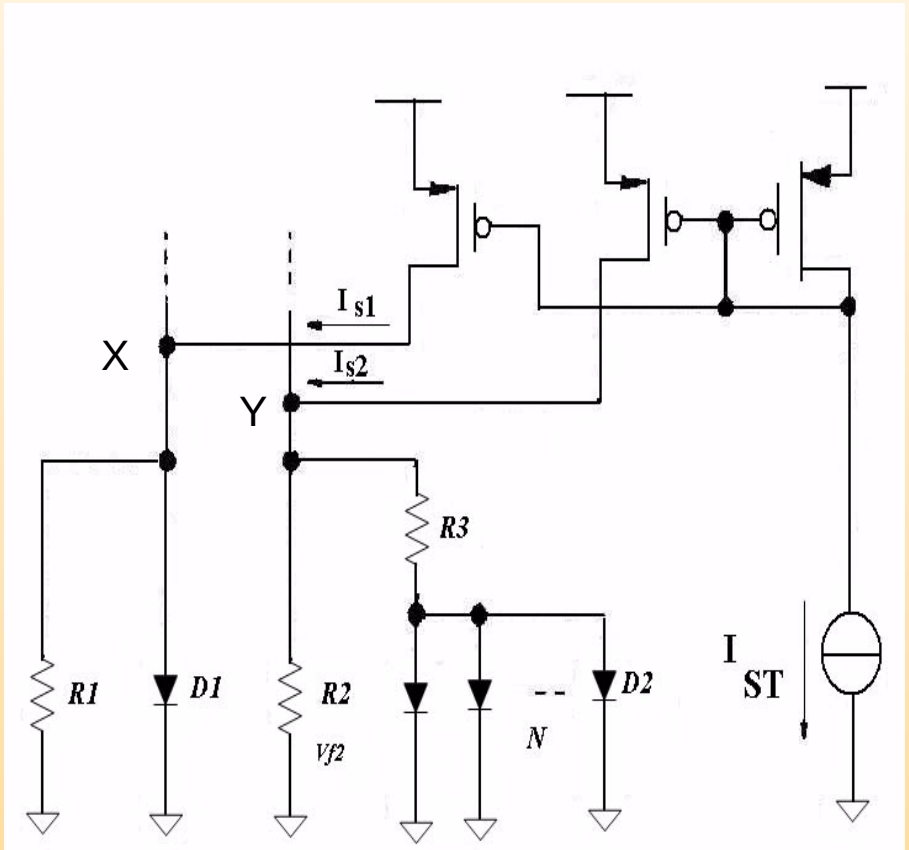

- Transistors **Q1** and **Q2** produce PTAT voltages across the resistors **R3** and **R2**.
- **Q3** drives the output to a voltage which is the sum of its **VBE** and the voltage across **R2.**
- When the output voltage is set to approximately the **bandgap voltage of silicon**, the voltage across **R2** will compensate the temperature coefficient of **VBE**, and the output voltage will have a **low TC.**

# Compatibility with CMOS Technology



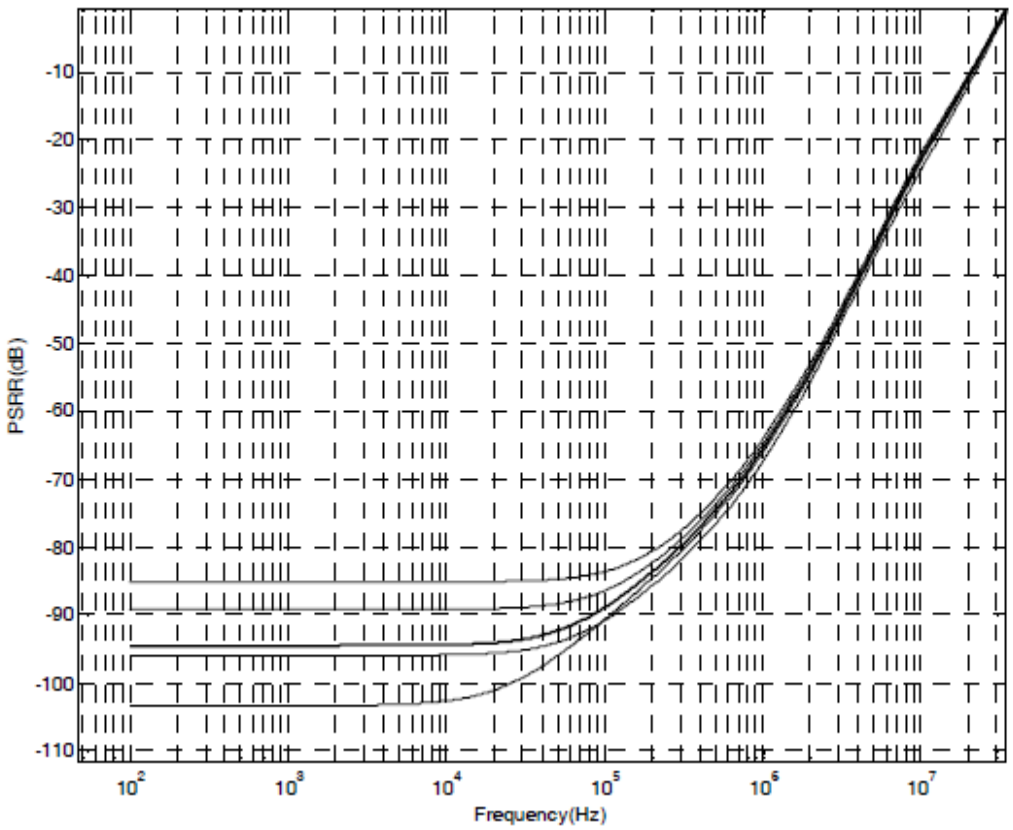

"parasitic" substrate PNP transistor
available in any CMOS technology

# Startup Circuit




- The BGR may settle at the power-on in stable operation point where the positive and negative input of the operational amplifier are at the ground potential
- This unwanted condition is avoided by the *startup circuit*

# PSRR




Power Supply Rejection Ratio (PSRR)

Bandgap core is supplied from a current source instead of voltage supply to have less dependency on power supply

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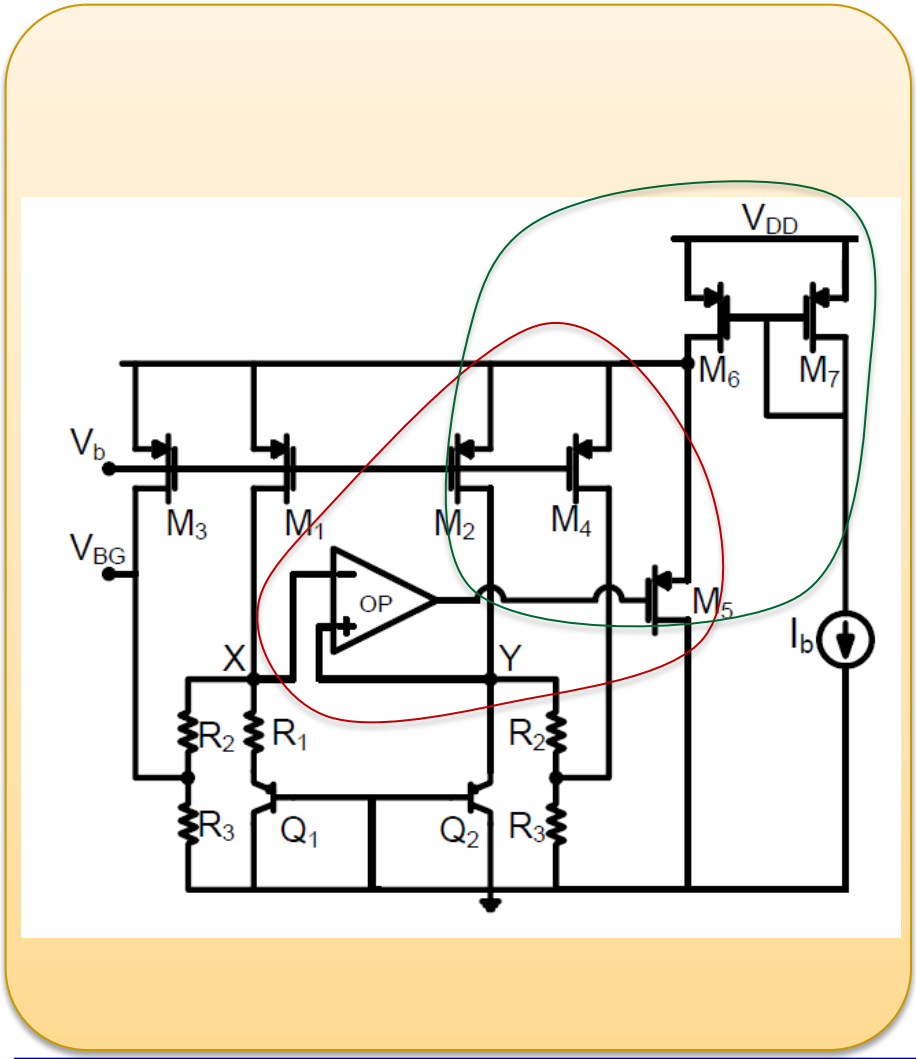
# High PSRR Mechanism




High PSRR is obtained by applying these strategies

- The bandgap core must supplied from regulated voltage made with a feedback loop
- The current reference that supplies the bandgap core designed wideband to have high PSRR, because the PSRR of this block is proportional to gain and bandwidth of Operational Amplifier

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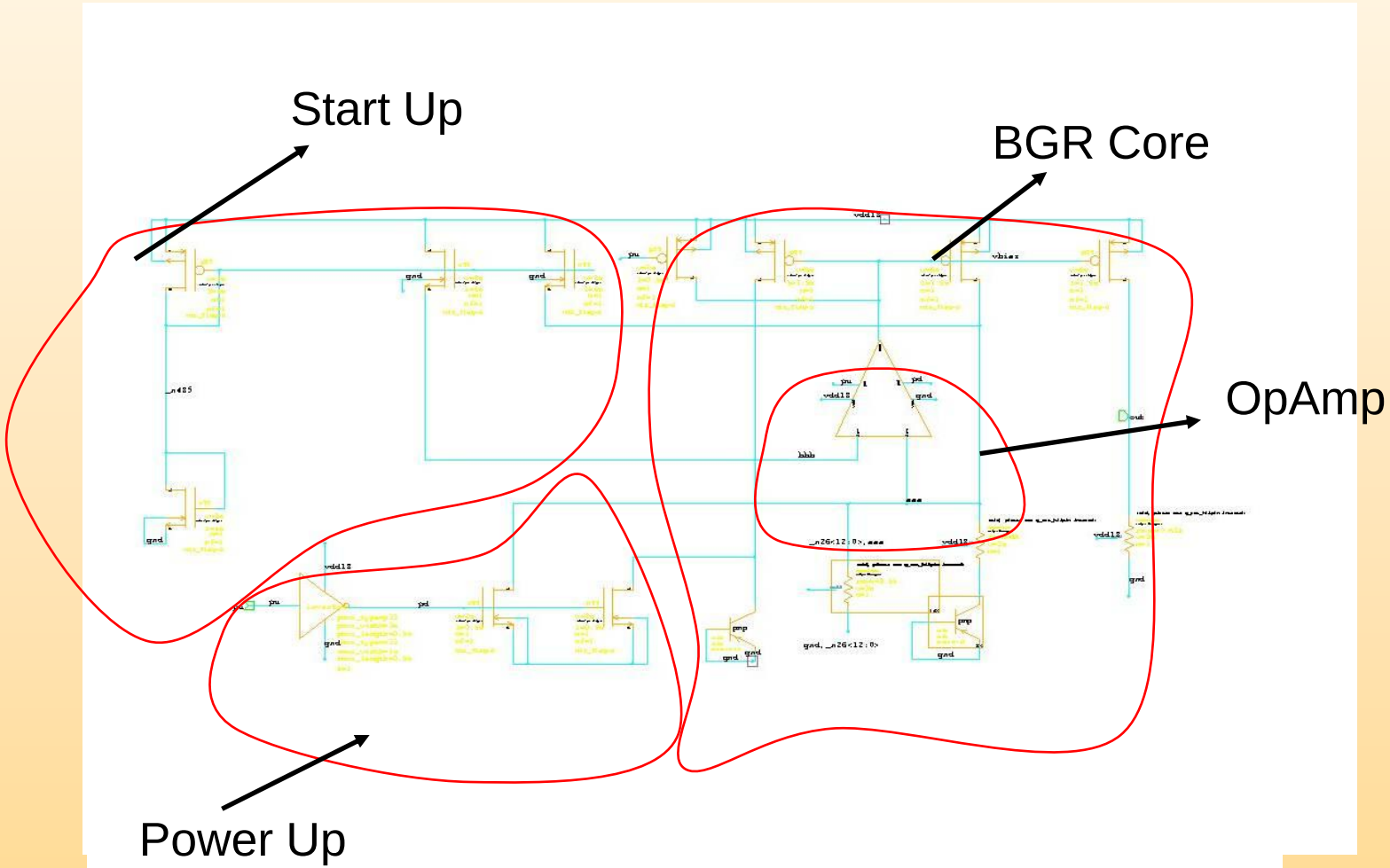
# Implemented Circuit

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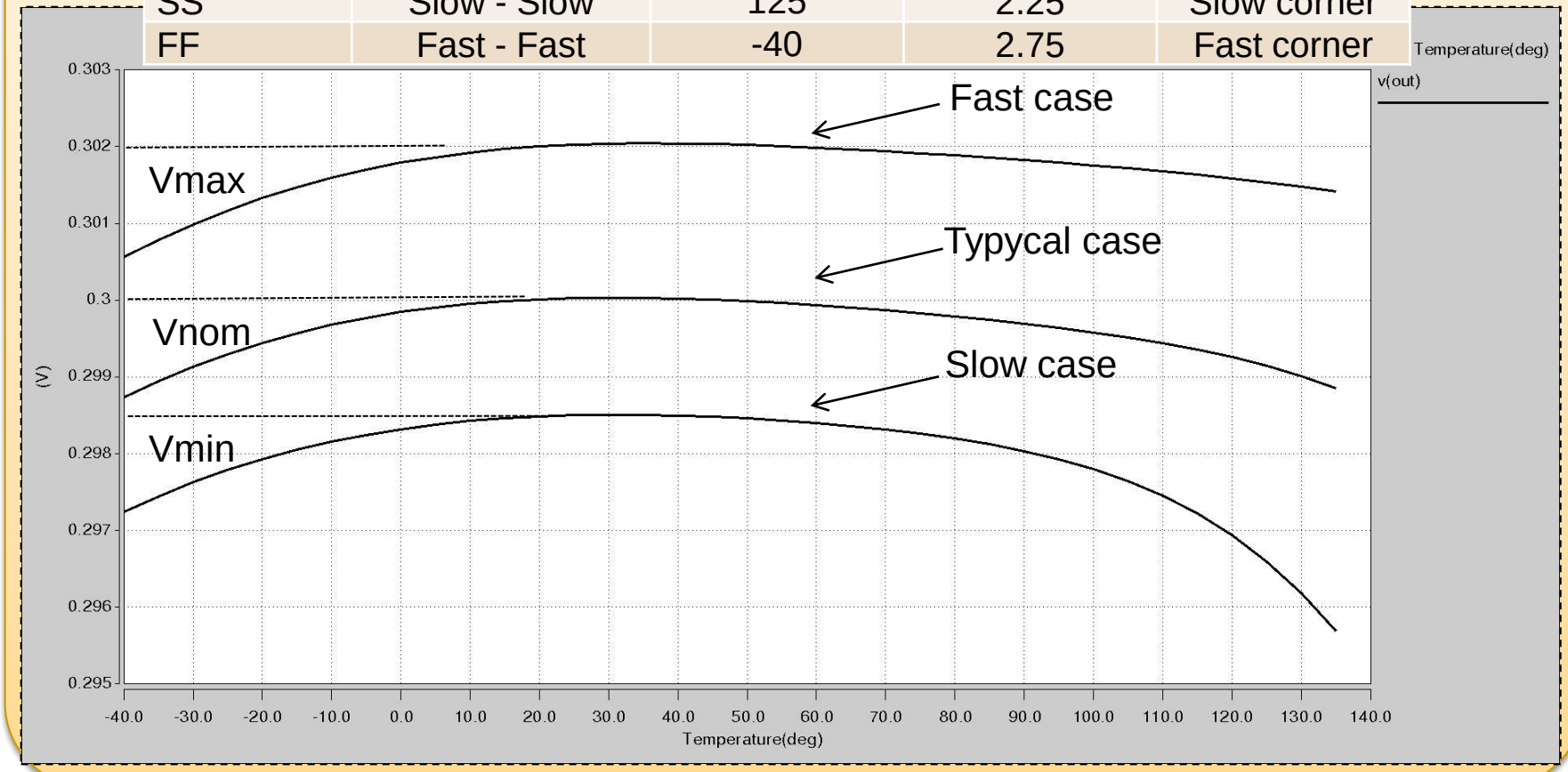
Why
Bell ?

# Temperature Dependence

| Corner Name | Process (NMOS proc. – PMOS proc.) | Temperature (T) | Power Supply (V) | Notes |
|---|---|---|---|---|
| TT | Typical - Typical | 25 | 2.5 | Typical corner |
| SS | Slow - Slow | 125 | 2.25 | Slow corner |
| FF | Fast - Fast | -40 | 2.75 | Fast corner |

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# Simulation Results

28nm technology

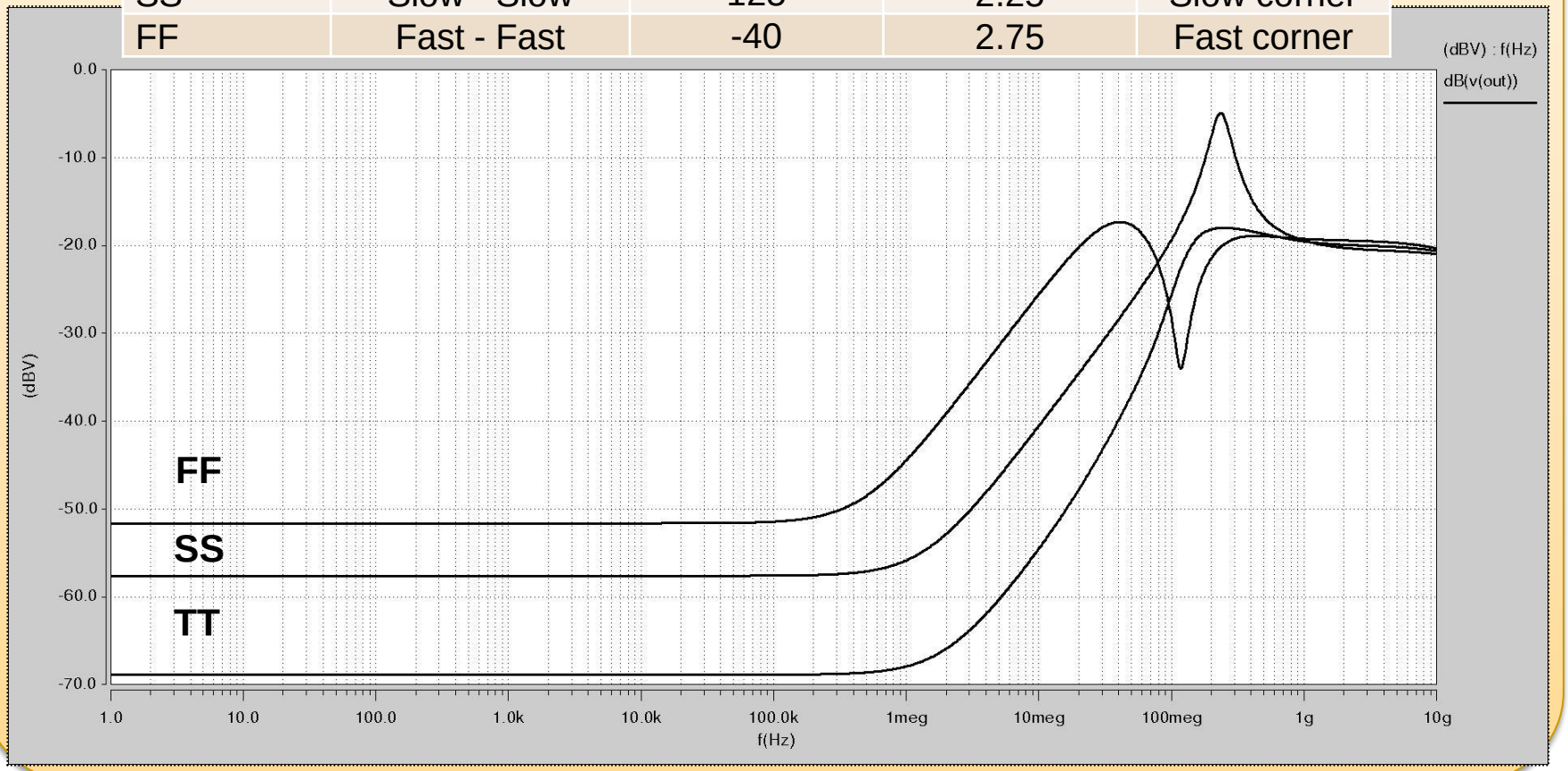
| | | | |
|---|---|---|---|
| TT | Typical case | 1.8V | 25 º C |
| SS | Worst case | 1.62V | 125 º C |
| FF | Best case | 1.98V | -40 º C |

Deviation (from above) = Vmax – Vnom/Vtyp=0.302 – 0.3 / 0.3 = 0.6%

Deviation (from below) = Vtyp – Vmin/Vtyp=0.3 – 0.296/ 0.3 = -1.33%

# PSRR for implemented circuit (1)

| Corner Name | Process (NMOS proc. – PMOS proc.) | Temperature (T) | Power Supply (V) | Notes |
|---|---|---|---|---|
| TT | Typical - Typical | 25 | 2.5 | Typical corner |
| SS | Slow - Slow | 125 | 2.25 | Slow corner |
| FF | Fast - Fast | -40 | 2.75 | Fast corner |

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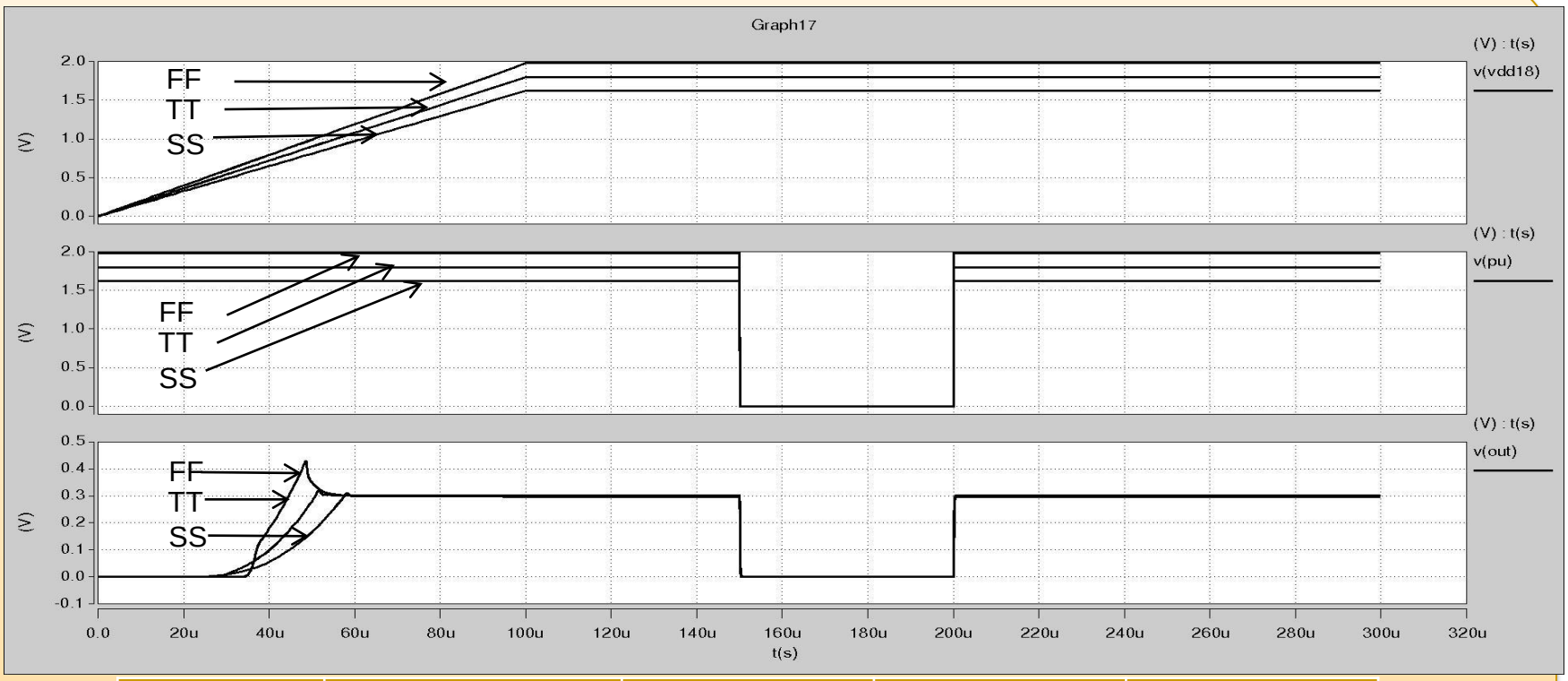
# PSRR for implemented circuit (2)

PSRR = 20 lg n

| | 1MHz | 10MHz |
|---|---|---|
| TT | -68.9 | -25.5 |
| SS | -51.6 | -40.5 |
| FF | -54.2 | -54.5 |

# Power Up and Power Down




| Corner Name | Process (NMOS proc. – PMOS proc.) | Temperature (T) | Power Supply (V) | Notes |
|---|---|---|---|---|
| TT | Typical - Typical | 25 | 1.8 | Typical corner |
| SS | Slow - Slow | 125 | 1.62 | Slow corner |
| FF | Fast - Fast | -40 | 1.98 | Fast corner |

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# Conclusion

Implemented 28nm  0.3V CMOS bandgap reference

## The Performance of the Bandgap Circuit

| Parameter | Measured |
|---|---|
| **Supply Voltage Range**<br>Vref<br>Vref Variation | 1.8 V +/- 10%<br>0.3 V<br>**+/- 1.45** |
| **Temperature Range**<br>Vref<br>Vref Variation | -40º C - 125º C<br>0.3 V<br>**+/- 1.33** |
| **PSRR**<br>Power Supply Rejection | 1-1GHz<br>Up to **70db 1Meg**<br>Up to **30db 10Meg** |

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Thank you